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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> <small>( Not for submission under 37 CFR 1.99)</small>	Application Number	10675872
	Filing Date	2003-09-30
	First Named Inventor	DeWitt, Jr. et al.
	Art Unit	2191
	Examiner Name	Vo, Ted T.
	Attorney Docket Number	AUS920030487US1

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Tu 1		6542985		2003-04-01	Johnson et al.	
Tu 2		4316245		1982-02-16	Luu et al.	
Tu 3		7181723		2007-02-20	Luk et al.	
Tu 4		6961925		2005-11-01	Callahan, II et al.	
Tu 5		5950003		1999-09-30	Kaneshiro et al.	
Tu 6		5212794		1993-05-18	Pettis et al.	
Tu 7		5659679		1997-08-19	Alpert et al.	
Tu 8		6006033		1999-12-21	Heisch	

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✓ 9	6119075		2000-09-12	Dean et al.	
✓ 10	6189141	B1	2001-02-13	Benitez et al.	
✓ 11	6237141	B1	2001-05-22	Holzie et al.	
✓ 12	6351844	B1	2002-02-26	Bala	
✓ 13	6505292	B1	2003-01-07	Witt	
✓ 14	6631514	B1	2003-10-07	Le	
✓ 15	5794028		1998-08-11	Tran	
✓ 16	5950009		1999-09-07	Bortnikov et al.	
✓ 17	5950003		1999-09-07	Kaneshiro et al.	
✓ 18	5581778		1996-12-03	Chin et al.	
✓ 19	5752062		1998-05-12	Gover et al.	

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<i>Tn</i>	20	6446029	B1	2002-09-03	Davidson et al.	
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<i>Tn</i>	1	20040194076	A1	2004-09-01	Comp et al.	
<i>Tn</i>	2	20020073406	A1	2002-06-13	Gove	
<i>Tn</i>	3	20030014741	A1	2003-01-16	Megiddo et al.	
<i>Tn</i>	4	20020157086	A1	2002-10-24	Lewis et al.	
<i>Tn</i>	5	20030040955	A1	2003-02-27	Anaya et al.	

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TZ	1	RAMIREZ et al., "The Effect of Code Reordering on Branch Prediction", Proceedings of the International Conference on Parallel Architectures and Compilation Techniques, October 2000, pp. 189-198.	<input type="checkbox"/>
TYL	2	YANG et al., "Improving Performance by Branch Reordering", Proceedings of the ACM SIGPLAN 1998 Conference on Programming Language Design and Implementation, Montreal Canada, 1008, pp. 130-141, 1998.	<input type="checkbox"/>
TCU	3	CONTE et al., "Accurate and Practical Profile-Driven Compilation Using the Profile Buffer", Proceedings of the 29th Annual ACM/IEEE International Symposium on Microarchitecture, Paris, France, 1996, pp. 36-45.	<input type="checkbox"/>
TYU	4	CONTE et al., "Using Branch Handling Hardware to Support Profile-Driven Optimization", Proceedings of the 27th Annual International Symposium on Microarchitecture, San Jose CA, 1994, pp. 12-21.	<input type="checkbox"/>
TYU	5	FISHER, "Trace Scheduling: A Technique for Global Microcode Compaction", IEEE Transactions on Computers, Vol. C30, No. 7, July 1981, pp. 478-490.	<input type="checkbox"/>
TYU	6	CHANG et al., "Using Profile Information to Assist Classic Code Optimizations", Software Pract. Exper. 21, December 1991, pp. 1301-1321.	<input type="checkbox"/>
TCU	7	SCHMIDT et al., "Profile-Directed Restructuring of Operating System Code", IBM Systems Journal, 1998, Vol. 37, No. 2, pp. 270-297.	<input type="checkbox"/>
TYU	8	AHO et al., "Compilers: Principles, Techniques, and Tools", Addison-Wesley, 1988, pp. 488-497.	<input type="checkbox"/>
TYU	9	INTEL, "Intel IA-64 Architecture Software Developer's Manual", Revision 1.1, Vol. 4, No. 245320.002, July 2001.	<input type="checkbox"/> July 2000

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TW	1	6105129		2000-08-15	Meier et al.	
TV	2	6928521	B1	2005-08-09	Burton et al.	
TV	3	6598153	B1	2003-07-22	Flachs et al.	
TV	4	5875294		1999-02-23	Roth et al.	
TV	5	6073109		2000-06-06	Flores et al.	
TV	6	6871298	B1	2005-03-22	Cavanaugh et al.	
TV	7	5555432		1996-09-10	Hinton et al.	
TV	8	6145077		2000-11-07	Sidwell et al.	

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<i>Tr</i>	9	6865666	B2	2005-03-08	Yoshida et al.	
<i>Tr</i>	10	5590352		1996-12-31	Zuraski et al.	
<i>Tr</i>	11	6199204	B1	2001-03-06	Donohue	
<i>Tr</i>	12	6202207	B1	2001-03-13	Donohue	

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<i>Tr</i>	1	20050257092	A1	2005-11-17	Alexander et al.	
<i>Tr</i>	2	20050177822		2005-08-22	Kuch et al.	
<i>Tr</i>	3	20030041096	A1	2003-02-27	Johnson	

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TIV	1	5657253		1997-08-12	Dreyer et al.	
TPV	2	5991708		1999-11-23	Levine et al.	
TPV	3	5564015		1996-10-08	Bunnell	
TPV	4	5450349		1995-09-12	Brown et al.	
TPV	5	5987598		1999-11-16	Levine et al.	
-TIV	6	6009514		1999-12-18	Henzinger et al.	
TPV	7	6112317		2000-08-29	Berc et al.	
TPV	8	5896538		1999-04-20	Blandy et al.	

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<i>TM</i>	9	5355487		1994-10-11	Keller et al.	
<i>TM</i>	10	6948032	B2	2005-09-20	Kadambi et al.	

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<i>TM</i>	1	"CPU Cache", Wikipedia, pp. 1-14 retrieved 11/1/06 <a href="http://en.wikipedia.org/wiki/CPU_cache">http://en.wikipedia.org/wiki/CPU_cache</a>	<input type="checkbox"/>
<i>TM</i>	2	AMMONS et al., "Exploiting Hardware Performance Counters with Flow and Context Sensitive Profiling", 1997, ACM, pp. 85-96.	<input type="checkbox"/>

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TV	3	6772322	B1	2004-08-03	Merchant et al.	
TV	4	5937437		1999-08-10	Roth et al.	
TV	5	6070009		2000-05-30	Dean et al.	
TV	6	6381679	B1	2002-04-30	Matsubara et al.	
TV	7	6687794	B2	2004-02-03	Malik	
TV	8	6539458	B2	2003-03-25	Holmberg	

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<i>Tu</i>	9	6973542	B1	2005-12-06	Schmuck et al.	
<i>Tu</i>	10	6782454	B1	2004-08-24	Damron	
<i>Tu</i>	11	5652858		1997-06-29	Okada et al.	
<i>Tu</i>	12	6848029	B2	2005-01-25	Coldewey	
<i>Tu</i>	13	5822790		1998-10-13	Mehrotra	

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TL	1	"Method for the dynamic prediction of nonsequential memory accesses", September 25, 2002, pp. 1-4, ip.com IPCOM000009888D	<input type="checkbox"/>
TL	2	"Cache Miss Director - A Means of Prefetching Cache Missed Lines", August 1, 1982, IBM Technical Disclosure Bulletin, Vol. 25, Issue 3A, pp.1286	<input type="checkbox"/>

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